Multiple input gates

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We were told in class that although in theory we can have multiple-input logic gate and therefore can get a two level implementation of functions, it is practically not possible. I don"t really understand why this is the case.

Individual gates are made up of series or parallel combinations of n or p channel transistors. The delay through the transistors is proportional to the total resistance of the transistors. This is worst case in CMOS technologies when you have a number of P channel transistors in series. Size for size P channel transistors have about 3 times more resistance than N channel. If they are all series you have a NOR gate.

The gate designer will attempt to increase the width of the P transistors in order to keep the rising propagation delay down. At some point it becomes more economical to use multiple gates to increase the effective number of inputs rather than increasing the transistor size in one gate.

Now repeat for 5 and more inputs : 5 inputs has a tiny advantage, 5N delay with a direct implementation, or 6N with the structure on the right. But perhaps you can see that at 8 inputs, the direct implementation is actually slower (8N) than the 6N implementation on the right.

There is a limit because any additional input requires an additional transistor and there is some voltage drop on the transistor which for a large number of transistors will be equal to the supply voltage.

Rule for an OR gate: output is "high" if input A or input B are "high."Rule for a NAND gate: output is not "high" if both the first input and the second input are "high."Rule for a NOR gate: output is not "high" if either the first input or the second input are "high."

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Web: https://sumthingtasty.co.za/contact-us/
Email: energystorage2000@gmail.com
WhatsApp: 8613816583346